**FSM**

**Verilog Module:**

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 12:05:37 01/24/2023

// Design Name:

// Module Name: FSM

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module FSM(open,Clk,Reset,in);

output open;

input Clk;

input Reset;

input in;

reg [1:0]next\_open;

reg [1:0]open;

reg [1:0]state;

reg [1:0]next\_state;

parameter [1:0]A = 2'b00;

parameter [1:0]B =2'b01;

parameter [1:0]C =2'b10;

always@(in or state)

begin

case(state)

A:begin

if(in) begin

next\_state=01;

next\_open=01;

end

else begin

next\_state=00;

next\_open=00;

end

end

B:begin

if(in) begin

next\_state=10;

next\_open=10;

end

else begin

next\_state=00;

next\_open=01;

end

end

C:begin

if(in) begin

next\_state=10;

next\_open=10;

end

else begin

next\_state=00;

next\_open=01;

end

end

endcase

end

always @(posedge Clk)

begin

if(Reset )

begin

state <= A;

open<=0;

end

else begin

state<=next\_state;

open<=next\_open;

end

end

endmodule

**TEXT FIXTURE:**

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 14:16:53 01/24/2023

// Design Name: FSM

// Module Name: C:/Xilinx/LabExam/LabExam/FSM\_TF.v

// Project Name: LabExam

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: FSM

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module FSM\_TF;

// Inputs

reg Clk;

reg Reset;

reg in;

// Outputs

wire [1:0]open;

// Instantiate the Unit Under Test (UUT)

FSM uut (

.open(open),

.Clk(Clk),

.Reset(Reset),

.in(in)

);

parameter PERIOD=100;

always

begin

Clk=1;

#(PERIOD/2);

Clk=0;

#(PERIOD/2);

end

initial begin

// Initialize Inputs

Reset = 1;

in = 0;

#100;

Reset=0;

in = 0;

#100;

in =0;

#100;

in =1;

#100;

in =1;

#100;

in =1;

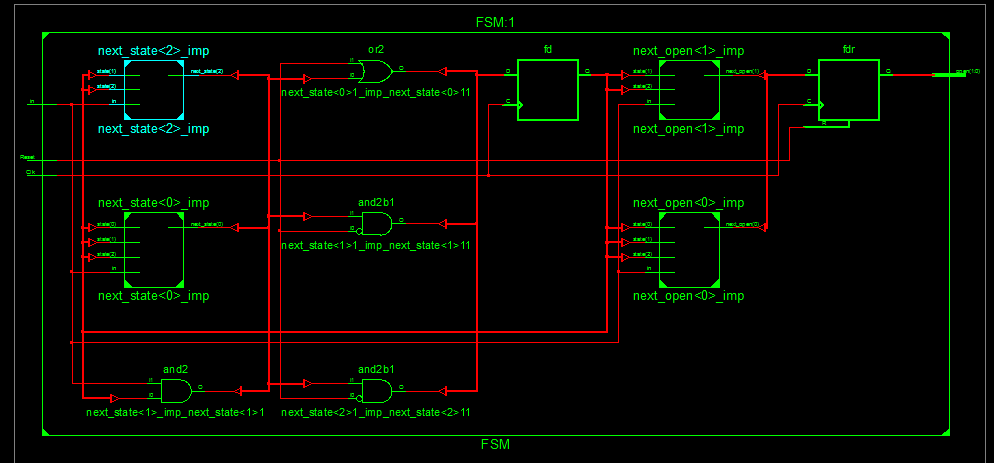
#100;

in =0;

#100;

end

endmodule

**SCHEMATIC:**

**WaveForm:**

